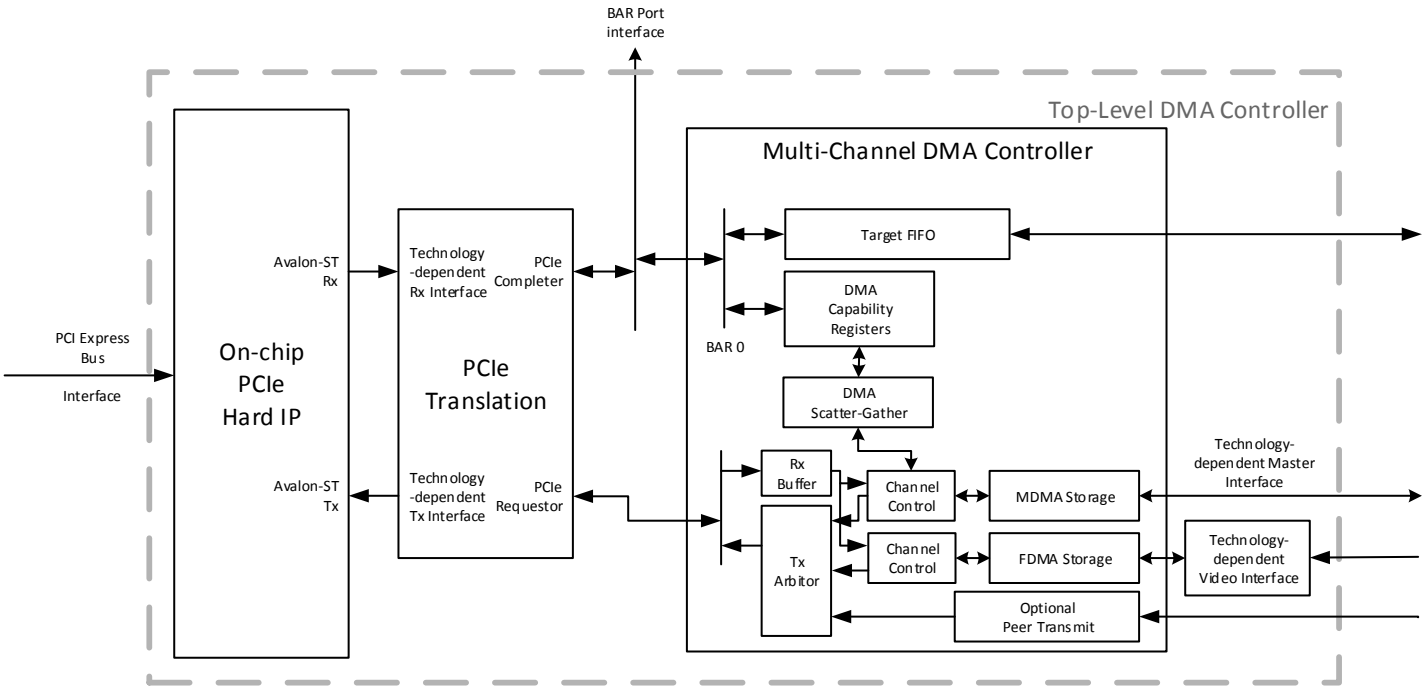
Multi-Channel Streaming DMA Controller – Xilinx® IP Core

Offering both memory-based 'MDMA' for handling transfers to and from addressed memory such as on-board SRAM and SDRAM, and FIFO-based 'FDMA' for streaming applications, Omnitek's DMA Controller and reference design applications provide the complete solution for rapid inclusion of fast PCI Express data transfers and streaming into Xilinx FPGA environments. Additionally, Omnitek's generic software API is platform-independent – enabling auto-discovery of applications and assists in providing a route to unique PCI identification of the final product.



Key Features

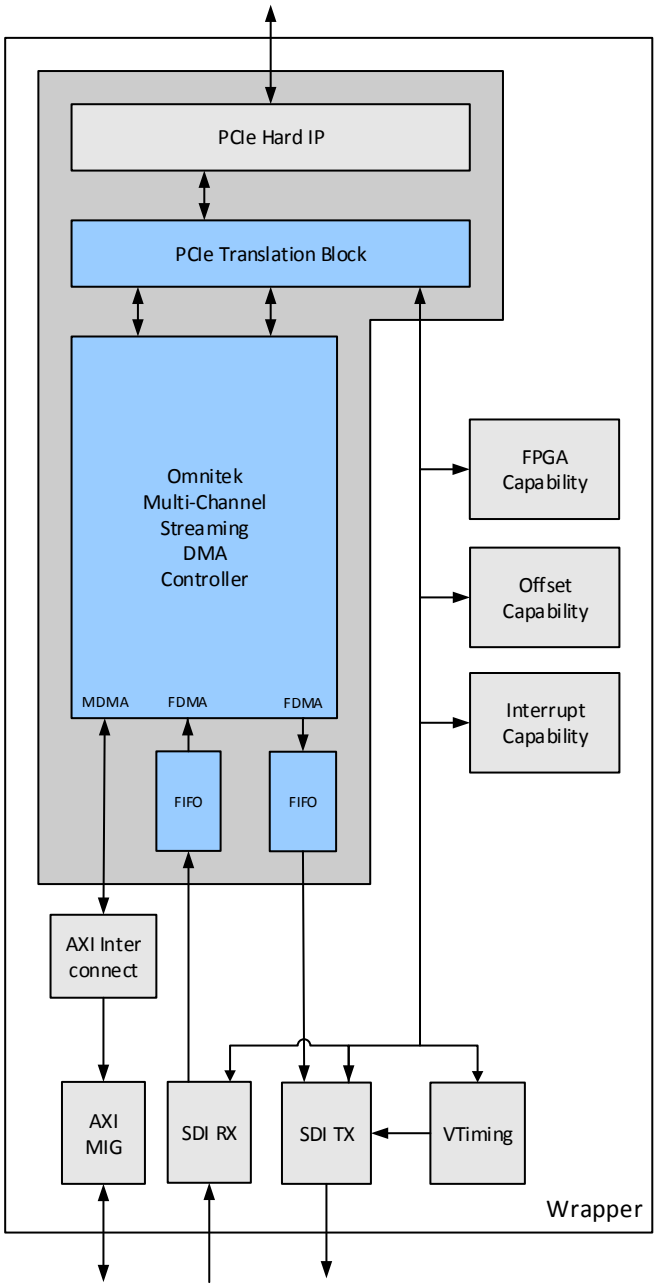
- PCIe-based DMA Controller firmware for Xilinx FPGAs
- Supports 7Series and UltraScale FPGA families
- Supports Vivado IP Integrator tool
- PCIe Gen1, Gen2, Gen3 support depending on FPGA family
- 1&2, 4 or 8 PCIe lane support options
- 64, 128 and 256-bit PCIe interface support
- PCIe 8lane Gen3 supports up to four UHDTV1 3840x2160p60 video streams.
- Offers both streaming FIFO-based DMA and memory-based DMA channels
- Highly efficient use of PCIe bandwidth, making it particularly suited to data streaming applications
- Support for multiple outstanding read requests
- Pre-fetching of Scatter-Gather descriptors for continuous streaming
- Optimised arbiter for back-to-back packing of TLP packets
- Optional Peer-to-Peer transfer support
- Configurable number of 32, 64 or 128bit FDMA streaming channels
- Supports 32-bit or 64-bit addressing
- Free 30-day evaluation

Deliverables

- Encrypted VHDL source code for DMA Controller Core IP
- Example Windows DirectShow application with compiled generic API and FPGA Debug, and also compiled drivers for Windows or source for Linux.
- Project file/wrapper supporting integration with compatible FPGA components
- Comprehensive documentation
- Technical Support and Maintenance Updates

Reference Design

The DMA Controller is delivered with a reference design that uses the DMA IP to create a video-streaming SDI – PCI Express bridge. The associated application demonstrates the ability of the DMA controller to simultaneously read and write multiple input video streams. It can work with SD, HD or 3G video. The application also demonstrates the use of the Windows driver and API supplied with the DMA Controller.



Typical resource use

	LUTs	Registers	Memory Blocks
Base DMA Controller	1261	1134	0
MDMA Channel (64 bits)	626	684	4
FDMA Input Channel (32 bits)	400	373	2
FDMA Ouput Channel (32 bits)	390	430	5
PCIe Translation Block (64 bits)	1864	1783	3

Licensing Options

Evaluation licence

- Fixed configuration version, available for free for 30 days through Omnitek website. Includes pre-compiled driver, Reference design and access to documentation (unencrypted).

Encrypted Source licence - NRE

- Allows IP to be compiled into designs.

Full Source Code licence

- Allows customisation of IP.

Product Options

- 1&2, 4 or 8 PCI Express Lane support
- Streaming (FIFO) FDMA support
- Number of DMA channels (up to 16)
- Peer-to-Peer support
- FPGA family
- QT application providing register/write DMA functions, source code
- Omnitek Generic API and Driver source code
- Extended evaluation period (over 30 days)
- Extended support period (over 1 year)

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