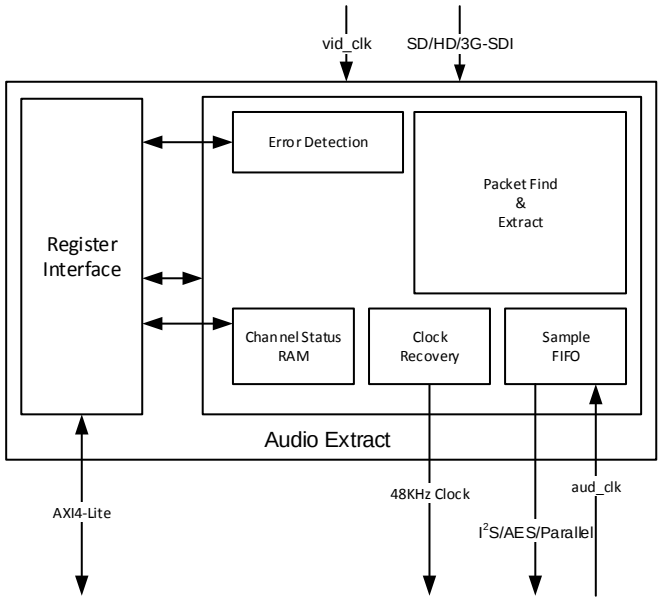
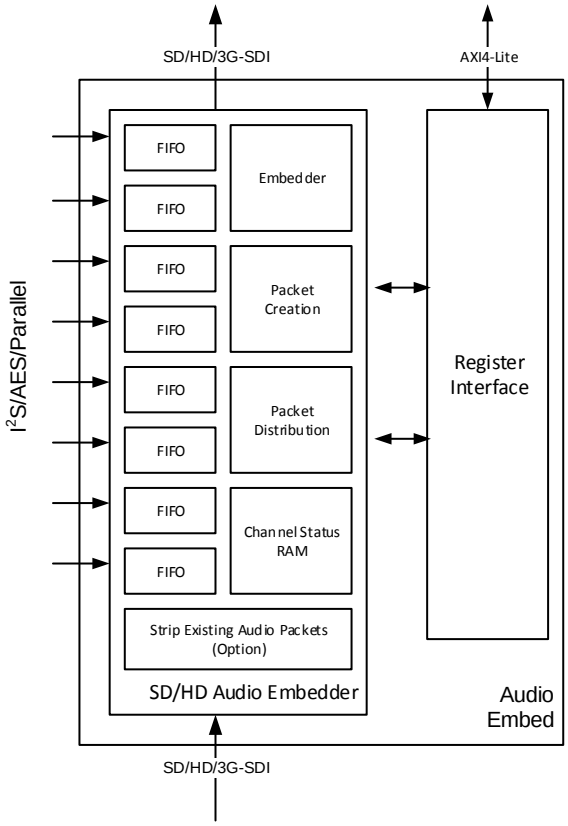
Audio Embed and Extract Components – Xilinx® IP Core

For embedding audio in SD/HD/3G SDI video and for extracting audio embedded in SD and HD SDI video.





Key Features

- Audio Embed/Extract firmware for Xilinx Virtex 5, Virtex 6, and 7-Series FPGAs or alternative technologies (if required)
- Handle audio conforming to SMPTE 272M (SD) or SMPTE 299M (HD/3G), presented as I²S Audio, AES Audio or Parallel Audio
- Support all sample rates permitted by the SMPTE standards
- Embed Block handles up to 16 channels (8 channel pairs); Extract block handles one channel pair but multiple blocks can be used together to handle the required number of channels
- Embed Block includes sine generator for test purposes
- Embed Block able to strip out existing audio
- Information reported by Extract Block includes which audio groups and control packets have been detected, a decode of the Audio Control Packet; and ancillary packet checksum, parity field and CRC error counts
- Both blocks controlled through set of slave registers accessed either through exposed ports or via optional register interface block
- Both blocks optionally available as source code in either Verilog or VHDL.
- Free 30-day evaluation option
- IP customisation and board development services also available

Deliverables

- Encrypted RTL or Source code for Audio Embed and Extract blocks
- Optional register interface
- Project file/wrapper supporting integration with compatible FPGA components
- Testbench
- Comprehensive documentation
- Technical Support and Maintenance Updates

Overview

The audio embedded by the Embed block is formatted either in accordance with the SMPTE272M standard (for SD video) or in accordance with the SMPTE299M standard (for HD and for 3G video).

The input audio may be at any of the sample rates permitted by the above SMPTE standards and can be provided in either I^2S Audio, AES Audio or Parallel Audio format. It can also be either synchronous or asynchronous to the video.

The Extract block is designed to extract both audio delivered as SMPTE272M packed data from standard definition SDI and audio delivered as SMPTE299M packed data from high definition SDI. The extracted audio may be output in either I^2S Audio, AES Audio, or Parallel Audio format.

The Embed block allows audio to be embedded in up to 16 channels (8 channel pairs). The Extract block is designed to extract audio from a single channel pair but multiple blocks may be used together to extract the audio from multiple channel pairs. Operations in both blocks are carried out in accordance with settings in associated sets of slave registers.

Licensing Options

Evaluation licence

- Available for free for 30 days through OmniTek website. Includes access to documentation (unencrypted).

Annual Encrypted IP licence

- Allows IP to be used in a production system.

Source Code licence

- Allows customisation of IP.

Product Options

- Audio Embed Block
- Audio Extract Block
- Annual Licence or Source Code
- FPGA family
- Extended evaluation period (over 30 days)
- Extended support period (over 1 year)

Typical resource use

Embed IP	LUTs	Registers	Memory
Embed block	385 + 465 per Audio Group (3 channel pairs)	390 + 345 per Audio Group	3 per Audio Group
Register Interface (optional)	55	100	0
Channel Status Memory (optional)	41 + 10 per Audio Group	25 + 10 per Audio Group	16 per Audio Group
Audio Clock generator (optional)	75	65	0
Sine Wave Generator (optional)	85	110	2
Stripper of existing audio (optional)	220 or 340	290 or 520	2 or 4

Extract IP	LUTs	Registers	Memory
Embed block	220	220	1
Register Interface (optional)	15	35	0
Channel Status Memory (optional)	32	25	1
Error Checking (optional)	176	125	0
FIFO Status (optional)	24	48	0
Clock Recovery (optional)	253	225	1

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